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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,108	07/31/2006	Eiji Ueda	2006-0816A	3708
52349 7590 03/25/2008 WENDEROTH, LIND & PONACK L.L.P. 2033 K. STREET, NW SUITE 800 WASHINGTON, DC 20006				
EXAMINER				
ELLS, KEVIN L				
ART UNIT		PAPER NUMBER		
2188				
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03/25/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/588,108

Applicant(s)

UEDA, EIJI

Examiner

Kevin L. Ellis

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SF/86)
Paper No(s)/Mail Date 7/31/06
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: ____

Detailed Action

1. Claims 1-10 are presented for examination.
2. Information disclosed and listed on PTO 1449 has been considered.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. § 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections – 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. § 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. The specification is objected to under 35 USC § 112, first paragraph, as failing to adequately teach how to make and/or use the invention, i.e. failing to provide an enabling disclosure.
6. The specification does not teach how the designated address can be different from an address to be processed by the reading unit and writing unit as stated in claim 5 when claim 1 sets forth that the reading unit and the writing unit only processes the designated address. Claim 1 limits the reading unit and writing unit to operate on the designated address. It is not clear then how the designated address can be different then the address processed by the reading and writing unit as stated in claim 5.
7. Claim 5 is rejected under 35 U.S.C. § 112, first paragraph, for the reasons set forth in the objection to the specification above.

Claim Rejections – 35 USC § 101

8. In claim 9, Applicant sets forth a "program for processing a storage unit", the body of the claim directed to the "program causing a computer to execute:". This claim is merely a program without being stored on a computer readable medium which can tangibly embody the program. Therefore this claim does not meet the "useful, concrete, and tangible" requirement as set forth in *State Street*, 149 F.3d at 1373, 47 USPQ2d at 1601-02, and hence claim 9 is not statutory under 35 U.S.C. 101.

Claim Rejections – 35 USC § 103

9. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 1-4 and 6-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tanitake, Japanese Patent Publication 2003-91988.

A) As to claim 1, Tanitake discloses the invention as claimed. There is a semiconductor memory card (Fig 8 Ref 20) comprising a first storage unit (Fig 8 Ref 25) operable to store data, the first storage unit having characteristics by which the data becomes uncertain in the first storage unit after the data is read (i.e. destructive read in the ferroelectric memory of Fig 8 Ref 25), a second storage (inside the control circuit Fig 1 Ref 4 or the CPU Fig 8 Ref 21) operable to store processing mode specific information

(i.e. should the data read be re-written or not) that specifies a mode of writing into each address of the first storage unit after the stored data is read out, a reading unit (inside the ferroelectric memory of Fig 8 Ref 25 there must comprise a reading unit) operable to read out the data stored in a designated address of the first storage, a processing mode determination unit (Fig 1 Ref 4) operable to determine the mode of writing into the designated address when the storage data is read out by the reading unit, and a writing unit (inside the ferroelectric memory of Fig 8 Ref 25 there must comprise a writing unit) operable to alternatively write or not write certain data into the designated address according to the mode determined by the processing mode determining unit (Fig 1 Ref 4) after the data stored in the designated address is read out.

There is an IC card (Fig 8 Ref 20) comprising a CPU (Fig 8 Ref 21), a ferroelectric memory (Fig 8 Ref 25), feedback section (Fig 1 Ref 3), and a control circuit (Fig 1 Ref 4). After a destructive read the control circuit decides whether or not the data read from the ferroelectric memory should be re-written back into the memory using the feedback section. For example, in the case of a "use-once" cryptographic key, the data are not rewritten so that an automatic erasing of data takes place i.e. the data becomes read once data (see ¶ 13, 132-134).

The IC card of Tanitake differs from the memory card of the present invention in that the mode of writing to the memory card into the designated address is determined by comparing the designated address with the processing mode specification information. It would have been obvious to have done similar with the system of Tanitake. For example, with the cryptographic key you would want to make the decision on whether or not to

rewrite the data based upon the address. Since the cryptographic key would be different for each cryptographic process, but the address where it was stored would be the same. Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to have based the decision upon whether or not the data is rewritten upon the designated address for the reasons given above.

- B) As to claims 2 and 4, the "certain data" can be read upon the data read from the memory.
- C) As to claim 3, it would have been obvious to one having ordinary skill in the art at the time of the invention to have used a random value to write to the designated address in the example of the cryptographic key. Since the key is a "use-once" the system could be assured that the value is destroyed by writing random data over the key once it's been read.
- D) As to claim 6, it would have been obvious to one having ordinary skill in the art at the time of the invention to have used a specified part of the designated address being used to determine the mode of writing. This would allow the system to partition the memory into areas that are destructive and non-destructive, the system would merely need to examine only a part of the address. For example, the lower half of the memory could be destructive and the top half non-destructive. By examining the most significant bit of the address the system would be able to determine if the address is in the destructive or non-destructive portion of the memory.
- E) As to claims 7-10, these claims recite the same features as those presented by claim 1 just directed to a method, integrated circuit, program, and a storage medium.

Accordingly they are similarly rejected. As for implementing the teachings of Tanitake as a program on a storage medium would have been obvious to one having ordinary skill in the art at the time of the invention. Implementing the system in software allows faster testing and debugging of the system.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin L. Ellis whose telephone number is 571-272-4205. The examiner can normally be reached on weekdays from 6:00AM-2:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone numbers for the organization where this application or proceeding is assigned is 571-272-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

/Kevin L. Ellis/
Primary Examiner
March 29, 2008